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PATENT COOPERATION TREATY

2858

From the INTERNATIONAL BUREAU

# PCT

## NOTIFICATION OF THE RECORDING OF A CHANGE

(PCT Rule 92bis.1 and Administrative Instructions, Section 422)

To:

CARPENTER, David
Marks & Clerk
Alpha Tower
Suffolk Street Queensway
Birmingham B1 1TT
ROYAUME-UNI

| | |
|---|---|
| **Date of mailing** (day/month/year)<br>09 January 2001 (09.01.01) | |
| **Applicant's or agent's file reference**<br>D036853PPC | **IMPORTANT NOTIFICATION** |
| **International application No.**<br>PCT/GB99/02060 | **International filing date** (day/month/year)<br>30 June 1999 (30.06.99) |

1. The following indications appeared on record concerning:

[X] the applicant [ ] the inventor [ ] the agent [ ] the common representative

| Name and Address | State of Nationality | State of Residence |
|---|---|---|
| MEM LIMITED<br>Turkey Shore<br>Holyhead<br>Anglesey<br>Gwynedd LL65 2DH<br>United Kingdom | GB | GB |
| | Telephone No. | |
| | Facsimile No. | |
| | Teleprinter No. | |

2. The International Bureau hereby notifies the applicant that the following change has been recorded concerning:

[X] the person [X] the name [X] the address [ ] the nationality [ ] the residence

| Name and Address | State of Nationality | State of Residence |
|---|---|---|
| DELTA ELECTRICAL LIMITED<br>1 Kingsway<br>London WC2B 6XF<br>United Kingdom | GB | GB |
| | Telephone No. | |
| | Facsimile No. | |
| | Teleprinter No. | |

RECEIVED JAN 22 2001 TECHNOLOGY CENTRE 2800

3. Further observations, if necessary:

4. A copy of this notification has been sent to:

[X] the receiving Office
[ ] the International Searching Authority
[ ] the International Preliminary Examining Authority
[ ] the designated Offices concerned
[X] the elected Offices concerned
[ ] other:

| | |
|---|---|
| **The International Bureau of WIPO**<br>**34, chemin des Colombettes**<br>**1211 Geneva 20, Switzerland** | Authorized officer<br>Christine Carrié |
| Facsimile No.: (41-22) 740.14.35 | Telephone No.: (41-22) 338.83.38 |

Form PCT/IB/306 (March 1994) 003759649

# PATENT COOPERATION TREATY

From the INTERNATIONAL BUREAU

## PCT

### NOTIFICATION OF ELECTION

(PCT Rule 61.2)

To:

Assistant Commissioner for Patents
United States Patent and Trademark Office
Box PCT
Washington, D.C.20231
ÉTATS-UNIS D'AMÉRIQUE

in its capacity as elected Office

| | |
|---|---|
| **Date of mailing** (day/month/year)<br>08 March 2000 (08.03.00) | |
| **International application No.**<br>PCT/GB99/02060 | **Applicant's or agent's file reference**<br>D036853PPC |
| **International filing date** (day/month/year)<br>30 June 1999 (30.06.99) | **Priority date** (day/month/year)<br>30 June 1998 (30.06.98) |
| **Applicant**<br>SKERRITT, Robert, Charles et al | |

1. The designated Office is hereby notified of its election made:

[X] in the demand filed with the International Preliminary Examining Authority on:

27 January 2000 (27.01.00)

[ ] in a notice effecting later election filed with the International Bureau on:

2. The election [X] was

[ ] was not

made before the expiration of 19 months from the priority date or, where Rule 32 applies, within the time limit under Rule 32.2(b).

| | |
|---|---|
| **The International Bureau of WIPO**<br>**34, chemin des Colombettes**<br>**1211 Geneva 20, Switzerland** | Authorized officer<br>Juan Cruz |
| Facsimile No.: (41-22) 740.14.35 | Telephone No.: (41-22) 338.83.38 |

Form PCT/IB/331 (July 1992)

3150143

# PATENT COOPERATION TREATY

From th
INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

To:

Marks & Clerk
Alpha Tower
Suffolk Street Queensway
Birmingham B1 1TT
GRANDE BRETAGNE



# PCT

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Rule 71.1)

| | |
|---|---|
| Date of mailing *(day/month/year)* | 02.10.2000 |
| Applicant's or agent's file reference<br>F036853PPC | **IMPORTANT NOTIFICATION** |

| International application No. | International filing date *(day/month/year)* | Priority date *(day/month/year)* |
|---|---|---|
| PCT/GB99/02060 | 30/06/1999 | 30/06/1998 |

Applicant
MEM LIMITED et al.

1. The applicant is hereby notified that this International Preliminary Examining Authority transmits herewith the international preliminary examination report and its annexes, if any, established on the international application.

2. A copy of the report and its annexes, if any, is being transmitted to the International Bureau for communication to all the elected Offices.

3. Where required by any of the elected Offices, the International Bureau will prepare an English translation of the report (but not of any annexes) and will transmit such translation to those Offices.

4. **REMINDER**

The applicant must enter the national phase before each elected Office by performing certain acts (filing translations and paying national fees) within 30 months from the priority date (or later in some Offices) (Article 39(1)) (see also the reminder sent by the International Bureau with Form PCT/IB/301).

Where a translation of the international application must be furnished to an elected Office, that translation must contain a translation of any annexes to the international preliminary examination report. It is the applicant's responsibility to prepare and furnish such translation directly to each elected Office concerned.

For further details on the applicable time limits and requirements of the elected Offices, see Volume II of the PCT Applicant's Guide.

| Name and mailing address of the IPEA/ | Authorized officer |
|---|---|
| European Patent Office<br>D-80298 Munich<br>Tel. +49 89 2399 - 0 Tx: 523656 epmu d<br>Fax: +49 89 2399 - 4465 | Baumann, H<br><br>Tel.+49 89 2399-2131 |

Form PCT/IPEA/416 (July 1992)

# PATENT COOPERATION TREATY

# PCT

REC'D 04 OCT 2000
WIPO PCT

## INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

US

| Applicant's or agent's file reference | FOR FURTHER ACTION | See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416) |
|---|---|---|
| F036853PPC | | |
| International application No. | International filing date *(day/month/year)* | Priority date *(day/month/year)* |
| PCT/GB99/02060 | 30/06/1999 | 30/06/1998 |
| International Patent Classification (IPC) or national classification and IPC<br>G01R19/00 | | |
| Applicant<br>MEM LIMITED et al. | | |

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 6 sheets, including this cover sheet.

   ☒ This report is also accompanied by ANNEXES, i.e. sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of 2 sheets.

3. This report contains indications relating to the following items:

   - I ☒ Basis of the report
   - II ☐ Priority
   - III ☐ Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   - IV ☐ Lack of unity of invention
   - V ☒ Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations suporting such statement
   - VI ☐ Certain documents cited
   - VII ☒ Certain defects in the international application
   - VIII ☐ Certain observations on the international application

| Date of submission of the demand | Date of completion of this report |
|---|---|
| 27/01/2000 | 02.10.2000 |
| Name and mailing address of the international preliminary examining authority:<br>European Patent Office<br>D-80298 Munich<br>Tel. +49 89 2399 - 0 Tx: 523656 epmu d<br>Fax: +49 89 2399 - 4465 | Authorized officer<br>Jakob, C<br>Telephone No. +49 89 2399 8948 |

Form PCT/IPEA/409 (cover sheet) (January 1994)

# INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No. PCT/GB99/02060

## I. Basis of the report

1. This report has been drawn on the basis of (*substitute sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to the report since they do not contain amendments.*):

**Description, pages:**

| | | | | |
|---|---|---|---|---|
| 1-7 | as originally filed | | | |

**Claims, No.:**

| | | | | |
|---|---|---|---|---|
| 1-7 | as received on | 28/07/2000 | with letter of | 24/07/2000 |

**Drawings, sheets:**

| | |
|---|---|
| 1/4-4/4 | as originally filed |

2. The amendments have resulted in the cancellation of:

☐ the description, pages:
☐ the claims, Nos.:
☐ the drawings, sheets:

3. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed (Rule 70.2(c)):

4. Additional observations, if necessary:

**V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement**

1. Statement

| | | |
|---|---|---|
| Novelty (N) | Yes: | Claims 1-7 |
| | No: | Claims |
| Inventive step (IS) | Yes: | Claims 5-7 |
| | No: | Claims 1-4 |
| Industrial applicability (IA) | Yes: | Claims 1-7 |
| | No: | Claims |

2. Citations and explanations

**see separate sheet**

**VII. Certain defects in the international application**

The following defects in the form or contents of the international application have been noted:

**see separate sheet**

**Section V.2**

1. The subject-matter of claims 1 to 7 is considered as new as required by Article 33(2) PCT for the following reasons:

1.1. The document US-A-5 701 253, which is cited in the International Search Report, is considered to represent the closest prior art and discloses a current detection device (see figures 1 and 2)

- comprising a plurality of resistive shunts (12a to 12c) for connection in respective ones of a plurality of lines (14a to 14c) through which current can flow to and from a load (16), and
- respective detector means (54, 51, 56) is provided for each shunt, each of the respective detector means being sensitive to the voltage developed across the shunt for providing a signal indicative of the current flowing through the shunt (column 4, lines 50 to 59).

1.2. The subject-matter of claim 1 differs from this current sensor in that it is destined for detecting residual current. Therefore the subject-matter of claim 1 and of the dependent claims 2 to 7 is considered as new (article 33(2) PCT and Rule 64.1 PCT).

2. Nevertheless, the subject-matter of claims 1 to 4 is not considered as involving an inventive step as required by Article 33(3) PCT for the following reasons:

2.1. Claim 1: As mentioned above, the claimed detection is destined for detecting residual current, whereas the device of the document US-A-5 701 253 is described in context with a power meter. The problem to be solved may therefore be regarded as how to provide the function of residual current detection to a device of the type described in document US-A-5 701 253.

In view of this problem, the skilled person would consider comparing the signals provided by the detector means (54, 51, 56) in order to detect an imbalance between the currents flowing through the shunts, e.g. by means

of the processor 60. The inclusion of such a feature in the device of the document US-A-5 701 253 is regarded as a straightforward design option which the skilled person would implement, in accordance with circumstances, without the exercise of inventive skill.

2.2. Claim 2: In the device of the document US-A-5 701 253, the detector means comprises an analog to digital converter (51, 56) for each shunt (24a to 24c) and a processor (60) for receiving the digital signals from the converters. Programming the processor such that it provides current imbalance detection is regarded as an obvious design approach.

2.3. Claim 3: Implementing the shunts as composite strips having conductive portions at their ends and an electrically resistive portion interconnecting the conductive portions is generally known in the art (cf. document EP-A-0 612 081 -cited in the International Search Report- in particular the abstract and figures 1 and 2).

2.4. Claim 4: Document US-A-5 701 253 discloses that the analog to digital converter (see e.g. figure 3, reference sign 100) for each shunt (12a to 12c) includes a delta-sigma modulator ('Δ-S ADC') which produces a high frequency signal digital data stream that is converted by decimation filtering into a multi-bit digital data stream at a lower frequency (cf. e.g. column 5, lines 30 to 41).

3. The dependent claims 5 to 7 are considered as inventive within the meaning of Article 33(3) PCT for the following reasons:

3.1. The subject-matter of claim 5 differs from the device of the document US-A-5 701 253 in that each converter is in the form of an integrated circuit mounted on a corresponding resistive shunt.

By mounting the converters on the shunts, the subject-matter of claim 5 provides a very compact current detecting device enabling a high immunity to perturbing interference.

3.2. Modifying the closest prior art such as to arrive at the subject-matter claimed was not obvious because none of the documents cited in the International Search Report indicates mounting an integrated circuit analog to digital converter on the associated shunt.

3.3. Since claims 6 and 7 depend on claim 5 in the sense of Rule 6.4(a) PCT, they too are considered as inventive within the meaning of Article 33(3) PCT.

4. The subject-matter of claims 1 to 7 meets the requirements of Article 33(4) PCT with respect to industrial applicability (see also the PCT Guidelines PCT/GL/3 IV, 4.1).

**Section VII**

1. Independent claim 1 of the application is not in the two-part form in accordance with Rule 6.3(b) PCT, which in the present case would be appropriate, since the features mentioned in section V.2. 1 above are known in combination from the document US-A-5 701 253 (see also the PCT Guidelines PCT/GL/3 III, 2.3a).

2. The features of the claims are not provided with reference signs placed in parentheses as required by Rule 6.2(b) PCT.

3. In claim 3, the signification of the expression "resist portion" is not clear (see also section V.2. 2.3).

4. Contrary to the requirements of Rule 5.1(a)(ii) PCT, the relevant background art disclosed in the documents US-A-5 701 253 and EP-A-0 612 081 (see sections V.2. 1 and 2 above) is not discussed in the description, nor are these documents identified therein.

5. The abbreviations "ASIC", "RCD", "ADC", "CPU" and "RMS" are not explained when being used for the first time in the application.

## CLAIMS

1. A residual current detection device for detecting current imbalance comprising a plurality of resistive shunts for connection in respective ones of a plurality of lines through which current can flow to and from a load, and respective detector means is provided for each shunt, each of the respective detector means being sensitive to the voltage developed across the shunt for providing a signal indicative of the current flowing through the shunt, whereby any imbalance between the currents flowing through the shunts can be detected.

2. A device as claimed in Claim 1, in which the detector means comprises an analog to digital converter for each shunt and a processor for receiving the digital signals from the converters and determining whether a current imbalance exists.

3. A device as claimed in Claim 1, in which each shunt takes the form of a composite strip having conductive portions at its ends and a resist portion interconnecting the conductive portions.

4. A device as claimed in Claim 2, in which the analog to digital converter for each shunt includes a delta-sigma modulator which produces a high frequency signal digital data stream which is converted by decimation filtering into a multi-bit digital data stream at a lower frequency.

5. A device as claimed in Claim 3, in which the analog to digital converter for each shunt includes a delta-sigma modulator which produces a high frequency signal digital data stream which is converted by decimation filtering into a multi-bit digital data stream at a lower frequency.

6. A device as claimed in Claim 2, in which each converter is in the form of an integrated circuit mounted on a corresponding one of the resistive shunts.

7. A device as claimed in Claim 6, in which each integrated circuit has analog input terminals connected by lead wires to the two copper end portions of the corresponding one of the resistive shunts.

8. A device as claimed in Claim 7, in which the integrated circuit also has a terminal connected to a voltage reference source and includes a second converter for providing a digital signal stream dependent on the voltage on one of the copper end portions of the associated one of the shunts.

9. A residual current detection device for detecting current imbalance comprising:

a plurality of resistive shunts for connection in respective ones of a plurality of lines through which current can flow to and from a load;

respective detector means provided for each shunt, each of the respective detector means being sensitive to the voltage developed across the shunt for providing a signal indicative of the current flowing through

the shunt, whereby any imbalance between the currents flowing through the shunts can be detected; and

means for providing at least one of additional function selected from a group comprising a conventional circuit breaker and a power consumption meter.

10. A residual current detection device for detecting current imbalance comprising:

a plurality of resistive shunts for connection in respective ones of a plurality of lines through which current can flow to and from a load;

respective detector means provided for each shunt, each of the respective detector means being sensitive to the voltage developed across the shunt for providing a signal indicative of the current flowing through the shunt, whereby any imbalance between the currents flowing through the shunts can be detected;

means for providing at least one of additional function selected from a group comprising a conventional circuit breaker and a power consumption meter; and

an analog to digital converter for each shunt and a processor for receiving the digital signals from the converters for determining whether a current imbalance exists.

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# PATENT COOPERATION TREATY

# PCT

## INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

| Applicant's or agent's file reference | FOR FURTHER ACTION see Notification of Transmittal of International Search Report (Form PCT/ISA/220) as well as, where applicable, item 5 below. | |
|---|---|---|
| D036853PPC | | |
| International application No. | International filing date *(day/month/year)* | (Earliest) Priority Date *(day/month/year)* |
| PCT/GB 99/ 02060 | 30/06/1999 | 30/06/1998 |
| Applicant | | |
| MEM LIMITED et al. | | |

This International Search Report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This International Search Report consists of a total of 2 sheets.

[X] It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

a. With regard to the **language**, the international search was carried out on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.

[ ] the international search was carried out on the basis of a translation of the international application furnished to this Authority (Rule 23.1(b)).

b. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international search was carried out on the basis of the sequence listing :

[ ] contained in the international application in written form.

[ ] filed together with the international application in computer readable form.

[ ] furnished subsequently to this Authority in written form.

[ ] furnished subsequently to this Authority in computer readble form.

[ ] the statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

[ ] the statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished

2. [ ] **Certain claims were found unsearchable** (See Box I).

3. [ ] **Unity of invention is lacking** (see Box II).

4. With regard to the **title**,

[X] the text is approved as submitted by the applicant.

[ ] the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,

[X] the text is approved as submitted by the applicant.

[ ] the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box III. The applicant may, within one month from th date of mailing of this international search report, submit comments to this Authority.

6. The figure of the **drawings** to be published with th abstract is Figure No. 1

[X] as suggested by the applicant.

[ ] because the applicant failed to suggest a figure.

[ ] because this figure better characterizes the invention.

[ ] Non of the figures.

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organizati n
International Bureau

(43) International Publication Date
12 July 2001 (12.07.2001)

PCT

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(30) Priority Data:
0000067.9 6 January 2000 (06.01.2000) GB

(71) Applicant *(for all designated States except US)*: **DELTA ELECTRICAL LIMITED** [GB/GB]; 1 Kingsway, London WC2B 6XF (GB).

(72) Inventors; and

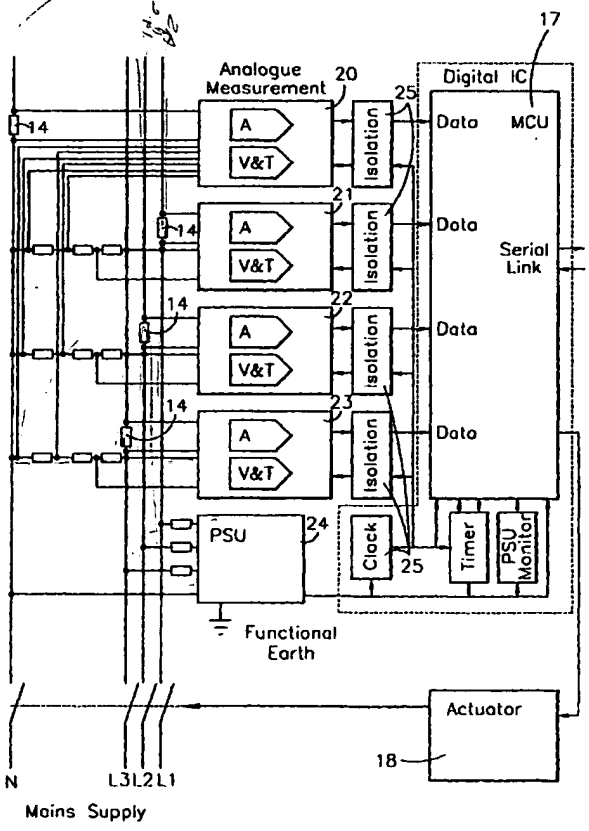
(75) Inventors/Applicants *(for US only)*: **SKERRITT, Robert, Charles** [GB/GB]; 2 Charleston Close, Penrhyn Bay, Conwy LL30 3HX (GB). **CROSIER, Mark, David** [GB/GB]; 4 Sunrise Terrace, Gors Avenue, Holyhead, Isle of Anglesey LL65 1PD (GB). **MURRAY, Martin, Anthony** [GB/GB]; 47 Penrhos Road, Bangor LL57 2AX (GB). **REEDER, Brian, Martin** [GB/GB]; "Samona", Lon Crecrist, Trearddur Bay, Isle of Anglesey LL65 2AZ (GB).

(74) Agents: **HACKETT, Sean, James** et al.; Marks & Clerk, Alpha Tower, Suffolk Street Queensway, Birmingham B1 1TT (GB).

(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW.

*[Continued on next page]*

(54) Title: CURRENT DETECTOR AND CURRENT MEASURING APPARATUS INCLUDING SUCH DETECTOR WITH TEMPERATURE COMPENSATION




(57) Abstract: A current sensing device and a residual current detection device are described having a temperature compensation capability so that residual current can be directly measured to a high degree of precision in the background of a high load current. The residual current device comprises a plurality of resistive shunts (14) for connection in respective ones of a plurality of lines through which current can flow to and from a load, and detector means (15) sensitive to the voltage developed across each of the shunts to detect any imbalance between the currents flowing through the shunts. The temperature compensation means (15h) is provided for facilitating compensation for fluctuations in shunt resistance with variations in temperature. The current sensor comprises a rigid metallic link member having two end portions (13) of conductive material and an intermediate portion (14) interconnecting the end portions. The intermediate portion is formed of a resistive material, and an integrated circuit analog to digital converter (15) is mounted on said link member. The converter has analog input terminals connected to respective ones of said two end portions and digital output terminals for connection to a processing apparatus. A temperature sensor (15h) is provided on or within said intermediate portion.

WO 01/50143 A1

(84) **Designated States** *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

**Published:**
— *With international search report.*

*For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*

# CURRENT DETECTOR AND CURRENT MEASURING APPARATUS INCLUDING SUCH DETECTOR WITH TEMPERATURE COMPENSATION

This invention relates to a current sensor with a temperature compensation capability intended for use in an electrical apparatus such as a residual current detection device.

It is an aim of the present invention to provide a current sensor capable of directly sensing current or voltage supplied to a load and a residual current detector in economical form which includes temperature sensing means for facilitating temperature compensation.

In accordance with the invention there is provided a current sensor comprising a metallic link member having two end portions of conductive material and an intermediate portion interconnecting the end portions, said intermediate portion being formed of a resistive material, and an integrated circuit analog to digital converter mounted on said link member, said converter having analog input terminals connected to respective ones of said two end portions and digital output terminals for connection to a processing apparatus, wherein a temperature sensor is provided on or within said intermediate portion.

The temperature sensor is preferably an electronic semi-conductor temperature sensor and may be mounted directly onto the intermediate portion with a thermally suitable or compatible conducting glue. The temperature sensor may be built into (i.e. integrated) into the integrated circuit analog to digital converter in which case it will form part of a semi-conductor die mounted directly onto the intermediate portion.

Embodiments of the invention have the advantage that the temperature sensor will follow the temperature of the intermediate portion very closely. It is therefore possible to compensate for changes in the resistance of the intermediate portion resulting from temperature variations as the current flowing therethrough changes.

Conveniently, the converter is attached to the intermediate portion by a layer of electrically insulative adhesive material and the analog input terminals of the converter are connected to the end portions by wire bonds.

The converter preferably includes a delta-sigma modulator which provides a high frequency one-bit digital data. One or more decimation filtering stages may be included in the converter.

The converter may also have a voltage reference terminal for connection to a reference voltage source, the converter operating to provide digital output signals respectively representing the current flowing through said intermediate portion and digital output signals representing the voltage on one of said end portions.

Embodiments of the invention may be advantageously employed in residual current devices. Conventionally, residual current is detected utilising a current transformer having primary windings through which, in the case of a single phase device, load current flows in opposite directions so that if the return current is different from the outwardly flowing current because of current leakage an output current signal is induced in a secondary winding of the transformer. In the case of a multi-phase device, primary windings of the transformer are connected in all of the phase lines and the neutral line. In

normal situations, when there is no current leakage, the net current induced in the secondary winding is zero and therefore no output is detected.

Sophisticated materials have been developed for the core of the current transformer, which enable considerable accuracy to be obtained when the currents flowing in the primary windings are substantially sinusoidal. However, switch mode power supplies are often used for computers and other equipment and there is an increasing tendency for such equipment to cause dc offsets in the currents. Such developments have made detectors utilising current transformers less reliable and prone to false tripping or failure to detect a dc current leakage.

This is a particular problem in the case of directly actuated electro-mechanical devices, where the current transformer secondary winding actually drives an actuator. The situation is not much improved, when including an electronic detection and amplification means connected to the secondary winding, as there are still problems with high frequency transients and dc offsets. A very small dc current level can cause the core to saturate thereby seriously impairing the ability of the detector to detect current leakage.

It is also an aim of the present invention to provide a residual current detection device in which the above mentioned problems are substantially overcome in a simple and efficacious manner.

In accordance with the invention there is further provided a residual current detection device comprising a plurality of resistive shunts for connection in respective ones of a plurality of lines through which current can flow to and

from a load, and detector means sensitive to the voltage developed across each of the shunts to detect any imbalance between the currents flowing through the shunts, wherein a temperature compensation means is provided for facilitating compensation for fluctuations in shunt resistance with variations in temperature.

In preferred embodiments, the temperature compensation means is a temperature sensor provided on or within each of said plurality of resistive shunts.

Preferably, the detector means comprises an analog to digital converter for each shunt and a processor for receiving the digital signals from the converters and determining whether a current imbalance exists. In this case, the temperature sensor may be built into (i.e. integrated) into the analog to digital converter. The temperature sensor is preferably an electronic semi-conductor temperature sensor mounted directly onto the shunt with a thermally conducting glue.

Each shunt preferably takes the form of a composite strip having conductive portions at its ends and a resistive portion interconnecting the conductive portions. Such composite strips can be mass produced inexpensively to very high tolerances which makes them extremely suitable for this purpose.

The analog to digital converter for each shunt may include a delta-sigma modulator, which generates a high frequency single-bit data stream which is converted by decimation filtering to a multi-bit digital stream at a lower frequency.

The analog to digital converter for each shunt is preferably connected to the processor through an isolation barrier so that the converter can float at the voltage level of the shunt which it serves. The decimation filtering may be effected entirely in the converter, entirely in the processor or split between the converter and the processor.

Embodiments of the invention provide for a high degree of accuracy in the measurement of the current and voltage in the circuit being monitored. It is desirable to measure the temperature of the current sensor for the purpose of compensating for changes in ambient temperature.

In order to detect residual currents of 1 to 10 mA in the background of a power supply current in the order of 100's of Amps, the degree of precision must be in the order of one part in 100,000. A useful residual current device is operative to detect residual currents in the order of a few to tens of mA, typically such that the circuit is tripped when the residual current detected reaches about 30mA. However, less sensitive residual current tripping thresholds can be set such as to trip at residual current levels as high as 100mA. This is a degree of precision several orders of magnitude greater than the degree of precision required for power metering applications and the like where it is sufficient to measure current to an accuracy of 1%. It is therefore advantageous to provide temperature compensation in accordance with embodiments of the invention in order to ensure accurate measurement of the residual current. In a preferred embodiment, the temperature of the current sensor is measured to an accuracy of plus or minus 0.25°C to plus or minus 0.5°C and the device may be calibrated over the expected temperature range, i.e. minus 5°C to 85°C.

Voltage measurement is required for power metering but a practical embodiment might measure to an accuracy of 1% although in a preferred embodiment, the voltage is measured to an accuracy of one part in about 1000 or better.

As each of the current, voltage and temperature are measured independently, it is possible to sense other functionalities such as one or more of power metering, current metering and arc fault protection. For example, abnormally high current measurements for extended periods may result from overloading, short circuits or line-to-ground faults and such events. Other events may also be detected, such as abnormal variations in current profile with respect to time. Such events may be indicative of faults which would not activate a residual current device. A wide variety of electrical characteristics are exhibited by at least some arcing faults and by monitoring the current and voltage with the precision afforded by embodiments of the invention, it is possible to detect situations where arc faults may be occurring. This monitoring may include detecting voltage drops indicative of arcing events or comparing the usual peak voltage of the circuit to the actual circuit voltage in the timed vicinity of the usual occurrence of the peak voltage. For example, peak voltages occur at 90 degree phase angles from the zero crossing point of the voltage. Voltage associated with the occurrence of an arcing fault is significantly reduced in the vicinity of the 90 degree phase angle.

The problem is that the energy levels of many arc short circuits is insufficient to trip many, if not all, conventional circuit breakers and some conventional fuses. By employing the current and voltage detection in embodiments of the invention, the current and voltage characteristic of the circuit can be

compared against prescribed criteria which represent arc fault conditions. The characteristics of arc faults are discussed in various publications of Underwriters Laboratories, Inc. (UL) including: "Technology For Detecting And Monitoring Conditions That Could Cause Electrical Wiring System Fires: Contract No: CPSC-C-94-1112, September 1995"; "The UL Standard For Safety For Arc-Fault Circuit Interrupters, UL1699, First Edition, dated February 26, 1999".

The invention will now be further described by way of non-limiting example with reference to the accompanying drawings, in which:

Figure 1 is a diagrammatic perspective view of an example of the invention as applied to a single phase device,

Figure 2 is a block diagram of another example of the invention as applied to a three phase device,

Figure 3 is a perspective view showing one of the current sensing devices embodying the present invention,

Figure 4 is a sectional view of the current sensing device of Figure 3,

Figure 5 is an elevation of the device of Figure 3,

Figure 6 is a block diagram of a simple form of the electronic circuit of a single current sensor device,

Figure 7 is a block diagram of an alternative form of the electronic circuit,

Figure 8 is a block diagram of yet another form of the electronic circuit, and

Figure 9 is a block diagram of a form of the electronic circuit which incorporates a temperature sensor in accordance with an embodiment of the present invention.

In the device shown in Figure 1, a substrate 10 supports two composite conductor strips 11, 12. Each of these includes end portions 13 of copper and an intermediate portion 14 of a resistive material such as manganin. The strips are formed by slicing up a sandwich formed by electron beam welding the copper portions to opposite sides of the manganin portion. The shunts formed by the resistive portions manufactured by this method can have a nominal resistance of 0.2mΩ to a tolerance of less than 5%. If the two shunts 14 used on one device are pressed from adjacent portions of the sandwich stock, they are matched to within 2%. Differences between characteristics of any two devices are predominantly linear. Hence, calibration of the shunts built into a unit at two different temperatures can virtually eliminate shunt errors. In this way, at least two temperature measurements are made. Two temperature measurements are taken because the difference in shunt A from shunt B is linear when the devices are adjacent to one another.

However, it is desirable to provide for direct compensation for temperature fluctuations arising from current fluctuations especially in a single current detector. The resistivity of an ideal precision resistance material is not changing with temperature. Compared to pure metals such as copper or aluminium with Temperature Coefficient of Resistance (TCR) values close to

4000ppm/DegC, the TCR values of Manganin or Zeranin are more than a factor of 400 better over the temperature of interest – but still not zero.

In reality, the plot of Resistance Vs Temperature (R(T) – curve) is not strictly linear and it is common practice to describe the curves by a third order polynomial. In general this is:

$R(T) = R_o * (1 + a_o * T + b_o * T^2 + c_o * T^3)$ where T = Temperature in DegC and $R_o$ = Resistance at 0 DegC.

At a more practical Reference Temperature of 20 DegC we can rewrite this as $R(T) = R_{20} * [1 + a_o * (T-20) + b_o * (T-20)^2 + c_o * T(-20)^3]$

The typical curves for the resistance materials Manganin and Zeranin curves are determined by the main composition of the alloys and vary very little from batch to batch. The production spread is less than 5 to 10ppm/DegC. These slight differences in the TCR value can be expressed in a tiny change of the first order coefficient "$a_o$" or "$a_{20}$" in the above equation and the second and third coefficients are basically not changed. For example a dR(T)/R20 – curve for different batches is just rotated around the 20 DegC point and the curve itself is unchanged. This explains the calibration of the shunts at two different temperatures mentioned above.

However in accordance with the present invention, it may be desired to calibrate each individual shunt in an RCD or in the case of the Current Sensor (Single Shunt) it could be calibrated separately. Varying as a third order polynomial at least 4 if not more points for a good calibration would be needed.

As described by the above equations if the temperature and our Ref resistance $R_{20}$ are known for example it is possible, with a suitable number of points, to find the coefficients and calibrate the shunt.

In the preferred embodiment, the temperature sensor itself (indicated generally by reference numeral 15h in figures 4 and 9) if built into (integrated) and is a part of the ASIC which includes the analogue to digital converter ADC. In other words the temperature sensor will be an electronic semi-conductor temperature sensor in the ADC. The ADC is mounted as a semi-conductor die directly onto the shunts with a suitable thermally conducting glue and will therefore track the temperature of the Manganin (shunt) very accurately.

Preferably, the temperature sensor output is sampled via the voltage modulator. It could have its own modulator (see RCD Fig 9 showing the added temperature channel) or be multiplexed into the voltage channel (see Fig 2).

For calibration it is possible to avoid having to make several stable temperatures to make the measurements. Instead a measurement can be made at 20 DegC for example and then a known current applied which heats up the shunts. Several measurements can be made during this process until the shunt arrives at its new steady state temperature as a result of the applied current.

In the example shown in Figure 1, there is a separate signal pre-processing ASIC 15 mounted on each of the shunts 14 and connected to the copper end

portions 13 of the associated conductor strips. The two ASICs 15 are connected to via an isolation transformer array 16 to a main processor 17. The ASICs 15 operate to convert the two voltages across the shunts into a digital signal stream which is communicated to the processor 17 via the isolation transformer array. The main processor is programmed to provide a drive signal to a trip actuator 18.

The actual preferred structural configuration of the current sensors is shown in Figures 3 to 5. These show leads 40 connecting two analog input terminals of the ASIC to the two copper end portions 13. Other leads connect other terminals of the ASIC 15 to a lead frame 40a by means of which all other external connections are made. Figure 5 shows in dotted lines a block 42 on encapsulation material and Figure 4 shows an electrically insulative adhesive layer 41 by means of which the ASIC is attached to the intermediate portion 14, which may be of manganin or zeranin of the composite strip 14, 15. The strips are formed by slicing up a sandwich formed by electron beam welding of the copper bars to opposite sides of a manganin bar. The temperature sensor is preferably integrated within the ADC of the ASIC 15.

Figure 6 shows that within the ASIC 15 there is provided a single delta-sigma modulator 15a. There is also an analog input circuit which has its input terminals connected to the copper end portions 13. The output of the ASIC 15 in this case consists of a high frequency one-bit data signal train. In use, the ASIC output is connected via a transformer or other isolation barrier 16 to a processor 17. The processor in this arrangement is configured to carry out one or more decimation filtering operations to convert the one-bit signal stream into a multi-bit value at a lower frequency.

The processor 17 may typically be configured to receive signals from a plurality of the detectors and to sum these signals to ascertain whether the current flows through the detectors are balanced. Such an arrangement can be used for residual current detection allowing an actuator to trip a switch if an unbalanced condition is found to exist. The processor 17 may alternatively or additionally compare the instantaneous current level with a trip level so that overcurrent tripping can be controlled.

Figure 2 shows in rather more electrical detail a three phase device. In this case there are four shunts 14, one in each phase line and a fourth in the neutral line. The ASICs 15 of Figure 1 are shown as four separate blocks 20, 21, 22 and 23, and there is a power supply unit 24 which draws power from the phase lines on the mains side of the shunts 14 and provides controlled voltages to the processor 17. Power is supplied to the four blocks 20 to 23 via isolation barriers 25 which make up the array 16. Each block of the ASIC includes an analog to digital converter in the form of a delta-sigma modulator which provides a high frequency one-bit digital data stream. A multiplexer may be included in each converter so that the converter can provide to the processor, through the respective isolation barrier, signals representing both current in the associated shunt and the voltage at one end of it. The processor, uses these signals to monitor the current in each shunt and to operate the actuator 18 if an imbalance occurs.

It will be noted that the voltage sensing connections to the ASICs are made via resistor chains connected between each phase line and the neutral. Each such resistor chain comprises an outer pair of precision resistors of relatively low ohmic value and an intermediate resistor of relatively high ohmic value.

These resistor chains allow the RCD to be provided with an independent reference. If the neutral ADC is taken as the selected system reference, then the operating software of the main processor can use the multiple signals derived from the several resistor chains to calibrate each phase against the neutral reference.

The CPU is programmed to carry out the necessary calculations to determine the existent of an imbalance and can determine the true RMS value of the residual current, which conventional devices fail to do correctly particularly in the case of non-sinusoidal current waveforms. The CPU may be programmed to enable it to determine from the data it receives whether a particular event is, in fact, an unacceptable leakage more reliably than conventional devices. For example, the CPU can take into account the historic performance of the unit when setting the leakage current threshold and may ignore events which have a recognisable "signature". In this way improved tolerance to nuisance tripping can be obtained.

Decimation filtering of the high frequency one bit data stream is required to reduce each data stream to a multi-bit digital signal at a predetermined sample frequency. By way of example, each current signal may be a 23-bit signal at a sample rate of 64 times the mains frequency, but lower resolution at lower sample rates can be employed when non-linear, rather than linear conversion is acceptable. The decimation filtering is typically a function of the processor, filtering of the four data streams being executed simultaneously so that sample values are derived for all four shunts simultaneously. A circuit employing such an arrangement is shown in Figure 6 as described above.

In an alternative embodiment as shown in Figure 7, one or more stages of the decimation filtration may be executed by hardware included within the ASIC. This includes a serial output driver 15b to transmit the bits of the multi-bit digital signal produced by the filtration stage 15c serially to the processor. Multi-bit digital words are transmitted serially across the isolation barriers instead of a one-bit signal stream. The filtration stages may be split between the ASIC and the processor. With this arrangement, the configuration of the processor can be simplified as part or all of the decimation filtration operation is carried out in the ASIC.

Where the current and voltage are both to be monitored as in the system shown in Figure 2, the circuit 15 may be as shown in Figure 8 with separate modulations and filtering components for the two signal streams and a common serial interface. Alternatively separate serial interfaces may be employed. The ASIC of Figure 8 has a further analog input which can be connected to a reference voltage source. Two analog input stages are present and these feed signals to two independent delta-sigma modulators 15d, 15e. As shown, there are two independent decimation filtration stages 15f, 15g for the two one-bit digital signal streams. The outputs of the stages 15f, 15g may, as shown be connected to a common serial output stage or (not shown) separate serial output stages may be provided.

It will be appreciated that the arrangement of Figure 8 may be modified by the omission of the two filtration stages 15f, 15g where all filtration is to be carried out by the processor.

Where voltage as well as current is monitored by the processor, precise calibration of the shunts can be achieved. This allows more accurate

determination of the current balance in RCD applications. Moreover, as voltage and current are both being monitored to a high level of precision, accurate power consumption metering can be obtained.

Where the devices of the invention are used in RCD and overcurrent trip systems, the processor can be programmed to recognise the transients which may occur when loads are switched in and out of circuit to avoid false tripping. Many other convenient functions can be programmed into the processor, made possible by the high precision of the current measurements capable of being carried out.

Figure 9 shows an arrangement similar to the one of Figure 8 except for the addition of a temperature sensor 15h in accordance with embodiments of the present invention. The temperature sensor 15h is input and sampled via the voltage modulator. The sensor could have its own modulator or be multiplexed into the voltage channel (Figure 9) as mentioned above. The arrangement of Figure 9 is operative to combine in a serial data stream the input parameters of current I, voltage V and temperature T.

The arrangements described enable very accurate detection of current imbalance to be effected even in the presence of switching transients and DC offsets. The problems which arise from potential saturation of the current transformer core are avoided completely.

Since the CPU receives actual line current and voltage data from each of the blocks 20 to 23, it can be programmed to perform other calculations, such as current limit and power consumption. Thus an RCD device constructed as described above can also provide the functions of a conventional circuit

breaker and/or those of a power consumption meter without any additional sensing or analog-to-digital components being required. The device may also be adapted to perform arc fault protection.

## CLAIMS

1. A residual current detection device comprising a plurality of resistive shunts for connection in respective ones of a plurality of lines through which current can flow to and from a load, and detector means sensitive to the voltage developed across each of the shunts to detect any imbalance between the currents flowing through the shunts, wherein a temperature compensation means is provided for facilitating compensation for fluctuations in shunt resistance with variations in temperature.

2. A device as claimed in Claim 1, in which the detector means comprises an analog to digital converter for each shunt and a processor for receiving the digital signals from the converters and determining whether a current imbalance exists.

3. A device as claimed in Claim 1 or Claim 2, in which each shunt takes the form of a composite strip having conductive portions at its ends and a resist portion interconnecting the conductive portions.

4. A device as claimed in Claim 2 or Claim 3, in which the analog to digital converter for each shunt includes a delta-sigma modulator which produces a high frequency single bit digital stream which is converted by decimation filtering into a multi-bit digital data steam at a lower frequency.

5. A device as claimed in Claim 2, 3 or 4, in which each converter is in the form of an integrated circuit mounted on a corresponding one of the resistive shunts.

6. A device as claimed in Claim 5, in which each integrated circuit has analog input terminals connected by lead wires to the two copper end portions of the corresponding one of the resistive shunts.

7. A device as claimed in Claim 6, in which the integrated circuit also has a terminal connected to a voltage reference source and includes a second converter for providing a digital stream dependent on the voltage on one of the copper end portions of the associated one of the shunts.

8. A current sensor comprising a rigid metallic link member having two end portions of conductive material and an intermediate portion interconnecting the end portions, said intermediate portion being formed of a resistive material, and an integrated circuit analog to digital converter mounted on said link member, said converter having analog input terminals connected to respective ones of said two end portions and digital output terminals for connection to a processing apparatus, wherein a temperature sensor is provided on or within said intermediate portion.

9. A current sensor as claimed in Claim 8 in which the converter is attached to the link member by means of a layer electrically insulating adhesive.

10. A current sensor as claimed in Claim 9 in which the converter is attached to the intermediate portion.

11. A current sensor as claimed in Claim 10 in which the analog input terminals of the converter are connected to the end portions by means of wire bonds.

12. A current sensor as claimed in any one of claims 8 to 11 in which the converter has a voltage reference terminal for connection to a reference voltage source and said converter operates to provide digital output signals representing the current through said intermediate portion and digital output signals representing the voltage on one of the end portions.

13. A current sensor as claimed in any one of claims 8 to 11 in which said converter includes a delta-sigma modulator which provides a high frequency one-bit digital data stream.

14. A current sensor as claimed in Claim 13 in which the converter also includes at least one decimation filter stage.

15. A current measurement apparatus including at least one current sensor as claimed in any one of claims 8 to 14 and a processor circuit connected to receive and process digital signals received from said current sensor.

16. A current measurement apparatus as claimed in Claim 15 in which the processor circuit is configured to carry out one or more decimation filtering operations on the received digital signals.

17. A current measurement apparatus according to any one of claims 8 to 16 or a residual current detection device according to any one of claims 1 to 7, wherein the temperature sensor is an electronic semiconductor temperature sensor mounted directly onto the intermediate portion or shunt with a thermally suitable conducting glue.

18. A current measurement apparatus or a residual current detection device according to Claim 17, wherein the temperature sensor is integrated into the integrated circuit analog to digital converter.

19. A current measurement apparatus or a residual current detection device according to any one of the preceding claims further comprising one or more of power metering, circuit breaking and arc fault protection.

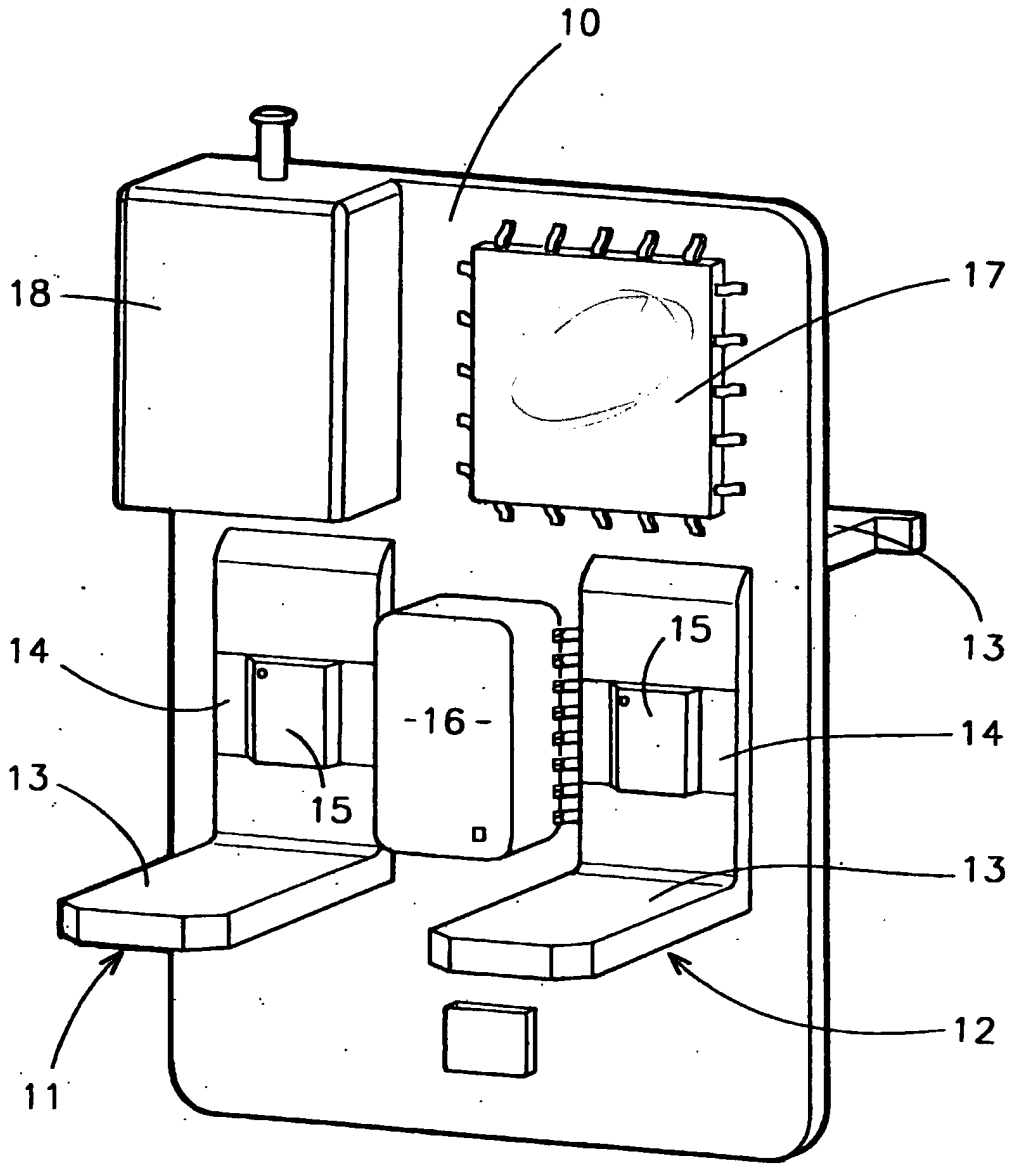



FIG 1

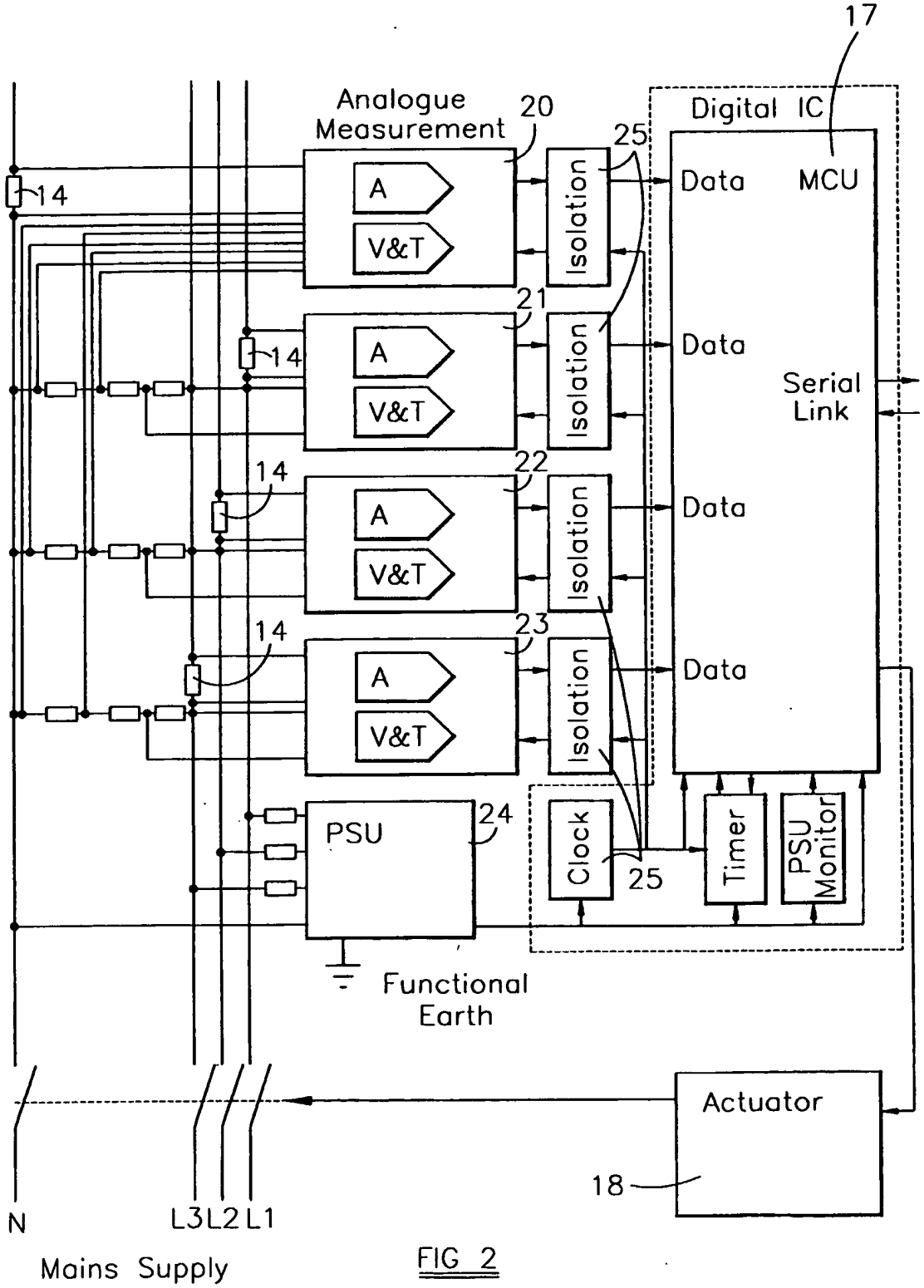

17
Digital IC
Analogue Measurement
20
25
Data
MCU
A
V&T
Isolation
14
21
Data
Serial Link
22
Data
23
Data
24
PSU
Clock
Timer
PSU Monitor
25
Functional Earth
Actuator
18
N
L3 L2 L1
Mains Supply

FIG 2

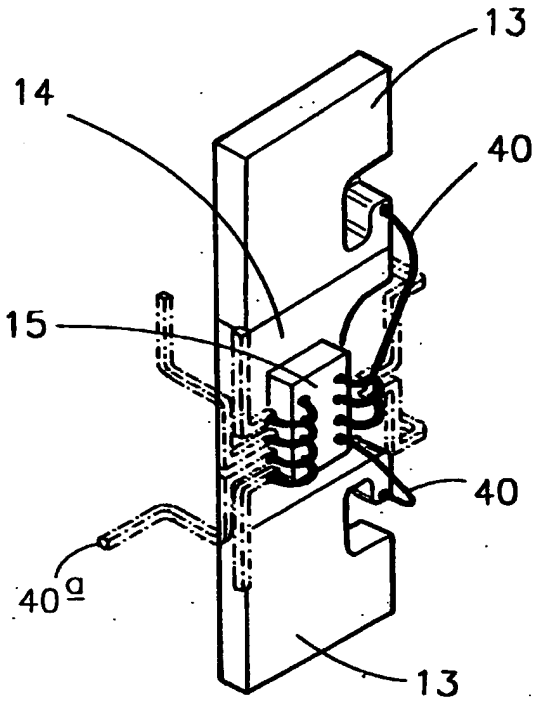



FIG 3

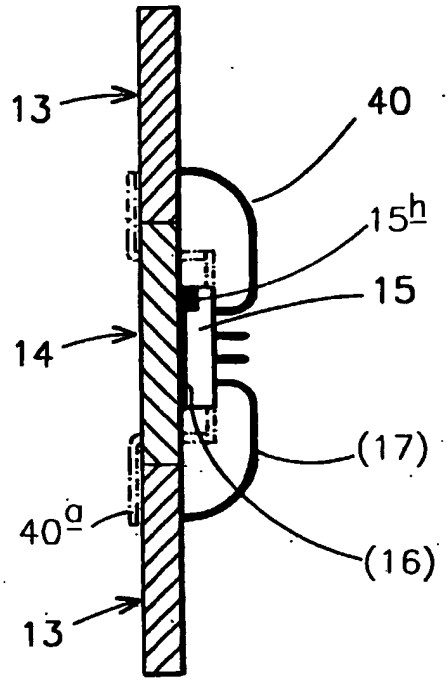



FIG 4

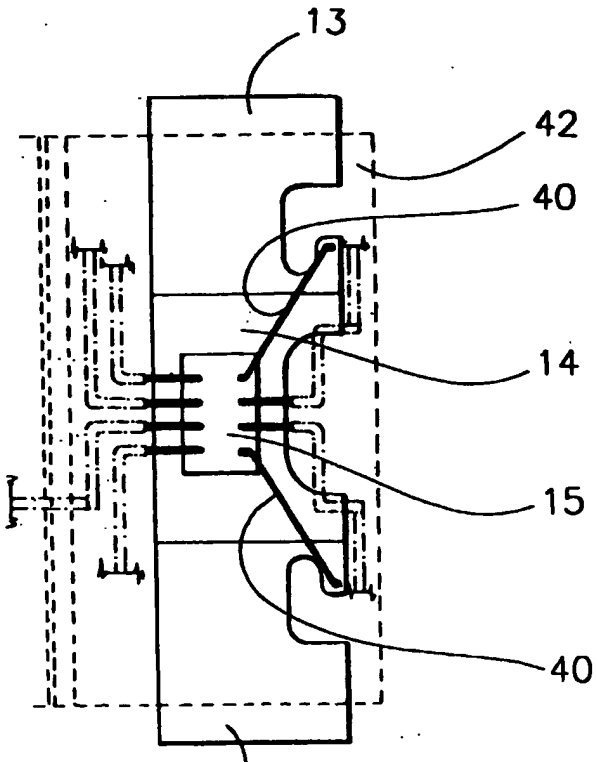



FIG 5

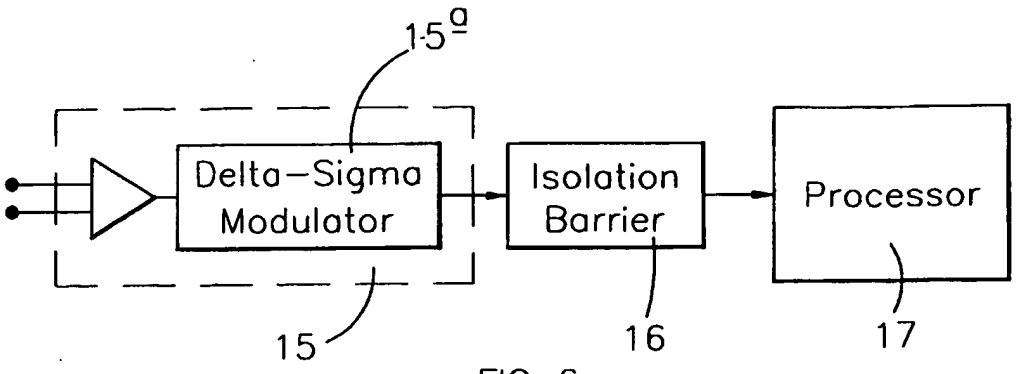



FIG 6

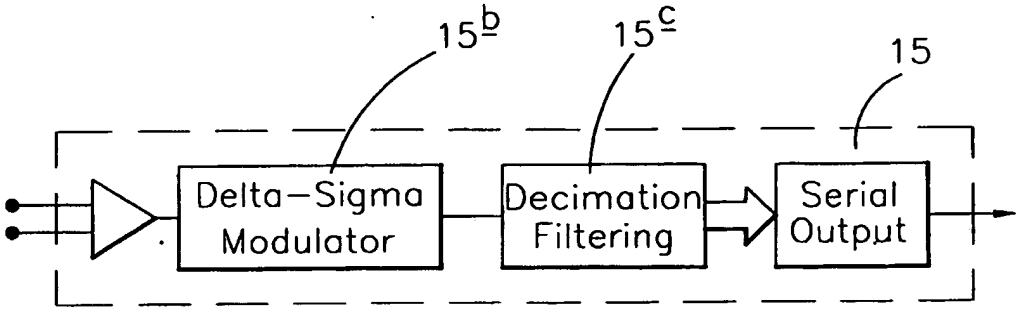



FIG 7

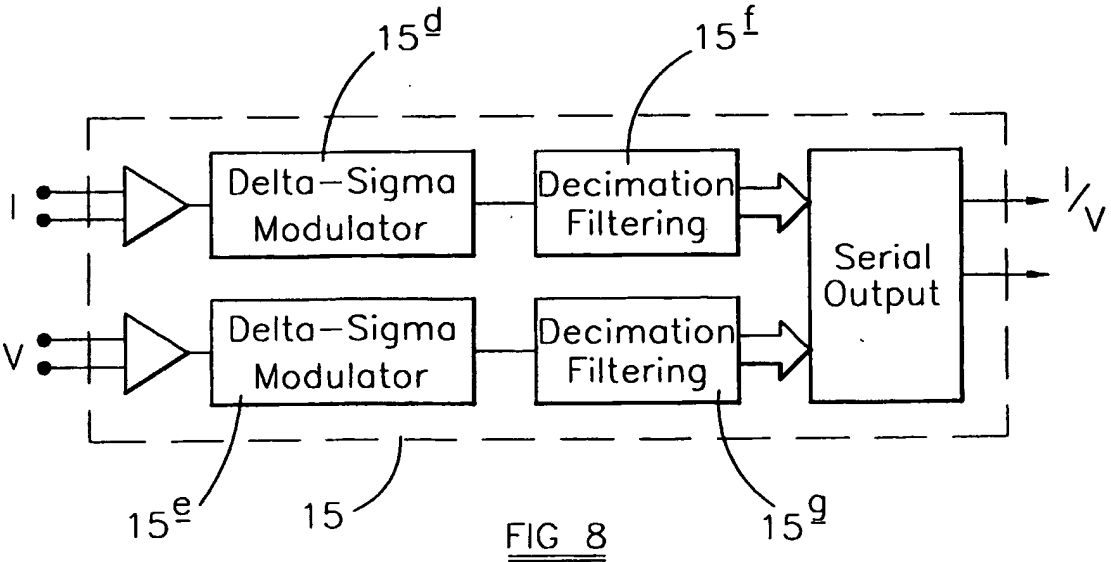



FIG 8

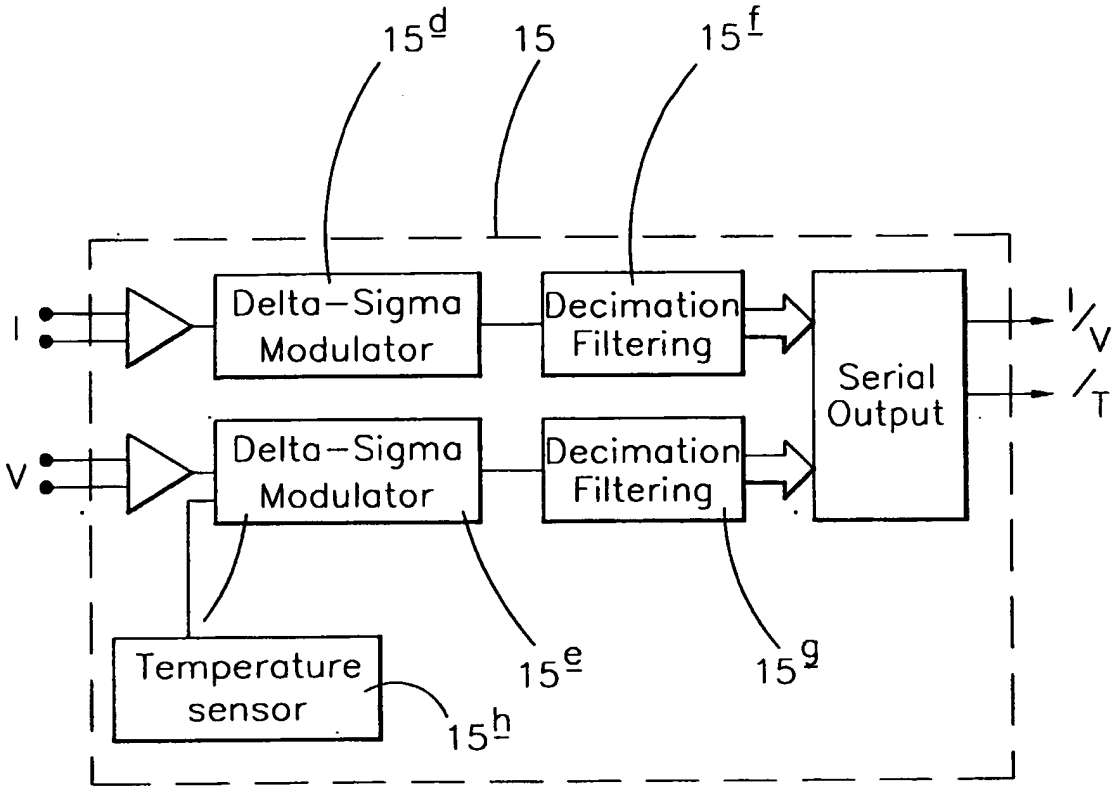

15d
15
15f
I
V
Delta–Sigma Modulator
Delta–Sigma Modulator
Decimation Filtering
Decimation Filtering
Serial Output
I/V
/T
Temperature sensor
15e
15g
15h

FIG 9

# INTERNATIONAL SEARCH REPORT

Inte I Application No
PCT/GB 01/00060

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G01R19/32

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G01R

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category * | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X | PATENT ABSTRACTS OF JAPAN vol. 016, no. 305 (P-1380), 6 July 1992 (1992-07-06) & JP 04 083175 A (MITSUBISHI ELECTRIC CORP), 17 March 1992 (1992-03-17) abstract | 1,8,17 |
| X | CA 2 244 692 A (STATPOWER TECHNOLOGIES CORP) 19 February 1999 (1999-02-19) the whole document & US 6 028 426 A 22 February 2000 (2000-02-22) | 1,8,17 |

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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"&" document member of the same patent family

| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 30 March 2001 | 10/04/2001 |

| Name and mailing address of the ISA | Authorized officer |
|---|---|
| European Patent Office, P.B. 5818 Patentlaan 2<br>NL - 2280 HV Rijswijk<br>Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,<br>Fax: (+31-70) 340-3016 | Six, G |

Form PCT/ISA/210 (second sheet) (July 1992)

# INTERNATIONAL SEARCH REPORT

Information on patent family members

Inter Application No
PCT/GB 01/00060

| Patent document cited in search report | Publication date | Patent family member(s) | Publication date |
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